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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

JC1114

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10046937	01/14/2002	326	725	2619	<i>[Signature]</i>

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KER VERDE

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

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PG-PLUS	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO H0002065
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		
Verified and Acknowledged Examiners's initials		
TITLE : Verification test method for programmable logic devices		

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED		
ISSUE FEE Amount Due Date Paid		Total Claims		Print Claim for O.G.
		DRAWING Sheets Drwg. Figs. Drwg. Print Fig.		
<input type="checkbox"/> TERMINAL DISCLAIMER		Assistant Examiner		
		Primary Examiner		
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE		
		Application Examiner		
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